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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,630	02/22/2002	Robert Yin	X-1070 US	4447

24309 7590 01/05/2005

XILINX, INC
ATTN: LEGAL DEPARTMENT
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EXAMINER

PERVEEN, REHANA

ART UNIT	PAPER NUMBER
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2116

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/082,630

Applicant(s)

YIN ET AL.

Examiner

Rehana Perveen

Art Unit

2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 1/04, 4/02.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11, 12, and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites the limitation "said at least one value" in line 3. There is insufficient antecedent basis for this limitation in the claim. Claims 12 and 13 are dependent of claim 11, and therefore, are also rejected for carrying the same lack of antecedent basis. Correction is therefore required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-6, 8-12, 15, 16, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lesea et al, Patent No. 6,496,971.

As to claims 1, 2, 4, 10, 11, and 12, Lesea et al teach pre-configuring an FPGA to a known state during a reset condition or prior to the FPGA undergoing system initialization (col. 6 lines 1-5), loading a configuration value for an on-chip device (col. 3 lines 1-12) of the FPGA into a flip-flop interconnected to the on-chip device (col. 6 lines 35-53 and col. 8 lines 33-43), pre-storing the configuration value in a memory cell (col. 6 lines 1-5), transferring the configuration value from the memory cell to the flip-flop upon power-up of the FPGA (col. 8 lines 33-40), and transferring the configuration value from the flip-flop to the on-chip device for effectuating pre-configuration of the on-chip device (col. 6 lines 1-9 and col. 8 lines 45-55).

As to claim 5, Lesea et al teach supplying a clock signal to the flip-flop to effectuate the transfer of the configuration value from the memory cell to the flip-flop upon power-up of the FPGA (col. 4 lines 26-65).

As to claim 6, Lesea et al teach supplying a clock signal to the flip-flop to effectuate the transfer of the configuration value from the flip-flop to the on-chip device (col. 4 lines 26-65).

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As to claims 8 and 9, Lesea et al teach the flip-flop is a configuration register (col. 10 lines 8-12), and the on-chip device is an on-chip memory controller (IC processor, col. 10 lines 50-67).

Claims 15, 16, 19, and 20 are directed to the system implementing the method of claims 1, 2, 4-6, and 8-12. Lesea et al teach the method as set forth in claims 1, 2, 4-6, and 8-12. Therefore Lesea et al also teach the system as set forth in claims 15, 16, 19, and 20.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 7, 14, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lesea et al, Patent No. 6,496,971.

Lesea et al teach all of the limitations as stated above. However, Lesea et al do not expressly teach the memory cell being a BRAM, the flip-flop being a D-type flip-flop, and the one value being a bit. Lesea et al disclose the method is performed using a memory cell (RAM) and a flip-flop but do not specify what type of memory cell or RAM and what type of flip-flop. The examiner takes official notice that BRAMs and D-type flip-flops are well-known types of random access memory and flip-flops, respectively.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention to use a BRAM and a D-type flip-flop for the random access memory and a flip-flop, respectively, for the system disclosed by Lesea et al. Also, Lesea et al do not address the exact bit-length. However, a bit length of one bit is well within the scope of the invention as Lesea has disclosed.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lesea et al, Patent No. 6,496,971, in view of Bertram et al, Patent No. 5,261,104.

Lesea et al teach all of the limitations as stated above. Lesea et al also teach storing the value for configuring the FPGA on-chip device in the at least one memory cell (col. 2 lines 33-42). However, Lesea et al do not expressly teach the stored value representing a default state of the memory cell. Bertram et al teach changing a default state of a configuration memory bits for controlling initialization routine at power-up, storing configuration value representing a default state of the configuration memory (col. 8 line 52 – col. 9 line 40).

It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Lesea et al and Bertram et al because both are commonly directed to pre-configuration environment for changing configuration values, and Bertram et al's controlling the default state, when incorporated into Lesea et al, would have enabled improved flexibility for the user to control the default state, thus enhancing system robustness.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rehana Perveen whose telephone number is 571-272-3676. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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